REMARKS

Summary of Office Action

Claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated by Onda (US 6,084,562).

Claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated by Eto et al. (US 5,301,031).

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Onda or Eto et al. in view of Sekido et al. (US 5,999,158).

Claims 1-7 stand objected to for allegedly reciting that "the reset signal is fed back and connected to the source shift clock."

Summary of Amendment

Claims 1, 3, 4, 6, and 7 were amended only to address minor informalities. Claims 1-7 are pending in this application for further consideration.

Claim Objections

It is noted that the previous amendments to independent claims 1 and 3, now objected to, were made as suggested by the examiner during a telephone conference of January 26, 2005 to place the application in condition for allowance. As the objections to claims 1 and 3 were considered to be minor informalities, claims 1 and 3 have been amended by adopting a portion of the Examiner's suggestions to now recite that "the reset signal is connected to a source shift clock source (emphasis added)" Support for this amendment can be found, for example, in Figure 7. Hence, no new matter has been entered. Applicants respectfully submit that these

amendments merely relate to correcting informalities and not any issues of patentability. Moreover, Applicants respectfully submit that these amendments do not narrow the scope of the claims.

All Claims Comply With §102 and §103

Claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated by Onda (newly cited), claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated by Eto et al. (newly cited), and claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Onda or Eto et al. in view of Sekido et al. (previously cited). These rejections are respectfully traversed because they do not establish a *prima facie* case of anticipation.

The Office Action alleges as to claims 1 and 3,

> ...Onda teaches an LCD display comprising the steps of: receiving a data enable signal (Vs) for indicating a time interval when a video data exists; detecting an enable initiation time of the data enable signal (Vs); generating a reset signal (VH) at the enable initiation time of data signals (Vs); resetting a source shift clock signal (CPH) for sampling video data (Vs') in response to the reset signal (VH) and the reset signal connected to a timing generating circuit (71) for generating a source shift clock signal (CHP). (OA: page 2, paragraph 3.)

Applicant respectfully disagrees. The rejection cites to Figures 1-5 and columns 5 and 6. In these sections, "Vs" is defined as a "video signal" (col. 5, lns. 42-43). "VH" is defined as a "horizontal sync signal" (col. 5, lns. 49). Therefore, Vs is not a "data enable signal" and "VH" is not a "reset signal" as alleged in the Office Action. Rather, Vs is the video signal itself (i.e., the video image data) that is inverted by the video signal inverting circuit based on the polarity signal POL (see Fig. 5). The VH (i.e., horizontal sync signal) serves to generate the start pulse signal (STH) as shown in Figures 3 and 4 and is not related to the horizontal shift clock (CPH).

Moreover, although Figure 5 illustrates the details of some of the internal components of control signal generating circuit 71, Figure 5 describes the control circuit 71 in relation to the "Y-driver circuit." In other words, Figure 5 of Onda shows the circuit for controlling ***vertical*** scanning (i.e., corresponding to the gate driver 64 of the present invention) and therefore is irrelevant to generating a "source shift clock," which is used for driving the "source driver IC" 66 of the present invention (i.e., corresponding to the X-driver circuit 13 of Onda). Indeed, Figure 5 illustrates a circuit for generating ***vertical*** clock (CPV) and ***not horizontal*** clock (CPH). As the signals of Onda do not correspond to the claimed method and components of claims 1 and 3 as asserted in the rejection, Applicant respectfully asserts that the rejection based on Onda fails to establish a *prima facie* case of anticipation.

Similarly, the Office Action alleges as to claims 1 and 3,

> ...Eto et al teach an LCD display comprising the steps of: receiving a data enable signal (1, R) for indicating a time interval when a video data exists; detecting an enable initiation time of the data enable signal (1, R); generating a reset signal at the enable initiation time of data signals (1, R); resetting a source shift clock signal for sampling video data (1, R) in response to the reset signal and the reset signal connected to a timing generating circuit (3) for generating a source shift clock signal (CKH). (OA: page 3, paragraph 4.)

Applicant again respectfully disagrees. The rejection cites to Figures 1-2 and columns 3 and 4. In these sections, Eto et al. defines "R" as a "picture signal" (col. 4, ln. 7) (i.e., the picture image information being captured into the sample and hold circuit 15 and applied to data lines i-th data line; col. 3, lns. 28-42). There is no mention of a "reset signal" or "resetting of a source shift clock." Accordingly, Applicant respectfully asserts that the rejection based on Eto et al. fails to establish a *prima facie* case of anticipation.

In addition to the rejection failing to establish a *prima facie* case of anticipation, Applicant respectfully asserts that Onda and Eto et al. both fail to teach or even suggest an apparatus and method for "detecting an enable initiation time of the data enable signal" and "generating a reset signal connected to a source shift clock source" for "resetting a source shift clock for sampling the video data" as recited, in part, in independent claims 1 and 3. As to dependent claims 2, 4, and 5, these claims depend, directly or indirectly, from corresponding base claims 1 and 3. Furthermore, Sekido et al. does not cure any of these deficiencies of Onda and Eto et al. Accordingly, Applicant respectfully requests that these rejections be withdrawn.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution. If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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By: _____

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